multiples thereof, the word length of the ALU being adjustable in accordance with the multiple of 8 bits constituting the integer ~~and~~ data words, the ALU having at least three operand inputs;

a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving the plurality of bits from the control register to execute the three port parametrised logic function;

a register unit provided with at least two registers for storage of the integer data words on which one of the operation and pipeline multiplication has to be performed; and

a bus structure for effecting the transport of integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit, the bus structure having a plurality of separate buses each having a separate register connected thereto for transmitting and receiving the integer data words.

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5. (Thrice Amended) An arithmetic logic unit having a varying word length for receiving and performing arithmetic operations on integer data words of varying length,

the word length of the arithmetic logic unit being automatically adjustable in accordance with the length of the integer data words being processed, the length of the integer data words being 8 bits or multiples thereof,

the ALU having at least three operand inputs and being capable of receiving a plurality of bits which define a three port parametrised logic function to be performed on the at least

three operand inputs and being capable of executing the three port parametrised logic function.

15. (Amended) A circuit for processing digital data words, comprising:

a multiplier unit for multiplying the digital data words, the multiplier unit having a pipeline in which the word length is adjustable to match the length of the digital data words, the digital data having a length of 8 bits or multiples thereof;

an arithmetic logic unit (ALU) capable of performing arithmetic operations on the digital data words, the ALU being adjustable to match the length of the digital data words, the ALU having at least three operand inputs;

a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving the plurality of bits from the control register to execute the three port parametrised logic function;

a register unit having at least two registers for storage of the digital data words; and

a bus structure for transporting the digital data words from and to the multiplier unit, the arithmetic logic unit and the register unit, the bus structure having a plurality of separate buses each having a register connected thereto for transmitting and receiving the digital data words.

21. (Amended) A circuit for processing digital data words, comprising:

a multiplier unit for multiplying the digital data words, the multiplier unit having a pipeline in which the word length is adjustable to match the length of the digital data words, the digital data words having a length of 8 bits or multiples thereof;

an arithmetic logic unit (ALU) capable of performing arithmetic operations on the digital data words, the ALU being adjustable to match the length of the digital data words, the ALU having at least three operand inputs;

24 a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving the plurality of bits from the control register to execute the three port parametrised logic function;

a register unit having at least two registers for temporary storage of the digital data words; and

a bus structure for transporting the digital data words from and to the multiplier unit, the arithmetic logic unit and the register unit, the bus structure including:

a first bus coupled to an output of the multiplier unit for receiving the digital data words therefrom;

a second bus coupled to an output of the arithmetic logic unit for receiving the digital data words therefrom;

third and fourth busses coupled to outputs of the two registers, respectively, for receiving the digital data words therefrom; and

a fifth bus coupled to the inputs of the multiplier unit, the arithmetic logic unit and the register unit for transmitting the digital data words thereto.

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22. (Amended) The circuit for processing digital data words of claim 15, further comprising a shift register unit operatively coupled to the ALU and being capable of receiving the digital data words having lengths of 8 bits or multiples thereof, the shift register unit for shifting the digital data words through a distance of 1 to multiples of 8 bits, in one of a left and a right direction and in one of a rotating and a non-rotating manner.

Please add the following new claim:

--25. An arithmetic logic unit capable of performing arithmetic operations on digital data words having a length which varies incrementally, the arithmetic logic unit being adjustable to match the length of the digital data words, the ALU having at least three operand inputs and being capable of receiving a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs and being capable of executing the three port parametrised logic function.--

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